AMENDMENTS IN THE CLAIMS:

1. (Currently amended) An integrated circuit comprising:

a substrate having interconnects ~~for~~ formed by an internal metallization layer and interconnecting integrated circuit devices;

a plurality of bond pads formed above the substrate; and

a first conductive trace formed by the internal metallization layer at an outer region of the substrate and coupled to at least two of the plurality of bond pads, the first conductive trace and at least two bond pads electrically isolated from the interconnects.

2. (Previously amended) The integrated circuit of Claim 1 wherein the first isolated conductive trace surrounds a plurality of bond pads.

3. (Previously amended) The integrated circuit of Claim 2 wherein the first isolated conductive trace has a chamfered region.

4. (Previously canceled without prejudice or disclaimer.)

5. (Previously amended) The integrated circuit of Claim 1 wherein the first isolated conductive trace comprises at least two separate first isolated conductive traces.

11. (Previously amended) The integrated circuit of Claim 10 further comprising a plurality of isolated conductive tester runners.

12. (Previously amended) The integrated circuit according to Claim 11 wherein at least two of the plurality of the isolated conductive tester runners having a varying height relative to an upper surface of the substrate.

13. (Previously amended) The integrated circuit of Claim 10 wherein the isolated conductive tester runner has a chamfered region.

14. (Previously canceled without prejudice or disclaimer.)

15. (Previously canceled without prejudice or disclaimer.)

6. (Previously amended) The integrated circuit according to Claim 5 wherein the at least two separate first isolated conductive traces have a varying height relative to an upper surface of the substrate.

7. (Previously amended) The integrated circuit according to Claim 1 wherein the first isolated conductive trace is formed at the periphery of the integrated circuit.

8. (Previously amended) The integrated circuit of Claim 1 wherein the first isolated conductive trace comprises at least two separate isolated conductive traces, each of the separate isolated conductive traces coupled to at least two of the plurality of bond pads.

9. (Previously canceled without prejudice or disclaimer.)

10. (Currently amended) An integrated circuit comprising:

a substrate having interconnects ~~for~~ formed by an internal metallization layer and interconnecting integrated circuit devices;

a plurality of bond pads formed above the substrate; and

a conductive tester runner formed ~~on the substrate~~ by the internal metallization layer and around the plurality of bond pads and electrically coupled to at least two of the plurality of bond pads, the conductive tester runner and at least two bond pads electrically isolated from the interconnects.